FERROELECTRIC CAPACITOR HYDROGEN BARRIERS AND METHODS FOR FABRICATING THE SAME

RELATED APPLICATIONS

5   This application is related to U.S. Patent Application Serial No. 10/620,516, filed on July 16, 2003, entitled "HYDROGEN BARRIER FOR PROTECTING FERROELECTRIC CAPACITORS IN A SEMICONDUCTOR DEVICE AND METHODS FOR FABRICATING THE SAME", and U.S. Patent Application Serial No. 10/635,994, filed on August 7, 2003, entitled "LOW

10   SILICON-HYDROGEN SiN LAYER TO INHIBIT HYDROGEN RELATED DEGRADATION IN SEMICONDUCTOR DEVICES HAVING FERROELECTRIC COMPONENTS", the entirety of these being hereby incorporated by reference as if fully set forth herein.

FIELD OF INVENTION

15   The present invention relates generally to semiconductor devices and more particularly to hydrogen barriers for protecting ferroelectric capacitors in a semiconductor device.

BACKGROUND OF THE INVENTION

20   Memory is used for storage of data, program code, and/or other information in many electronic products, such as personal computer systems, embedded processor-based systems, video image processing circuits, portable phones, and the like. Memory cells may be provided in the form of a dedicated

25   memory integrated circuit (IC) or may be embedded (included) within a processor or other IC as on-chip memory. Ferroelectric memory, sometimes referred to as "FRAM" or "FERAM", is a non-volatile form of memory commonly organized in single-transistor, single-capacitor (1T/1C) or two-transistor, two-capacitor (2T/2C) configurations, in which each memory cell includes one or more access

30   transistors. The non-volatility of an FERAM is due to the bi-stable characteristic

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of the ferroelectric material in the cell capacitor(s). The cells are typically organized in an array, such as folded-bitline, open-bitline architectures, etc., wherein the individual cells are selected by plateline and wordline signals from address decoder circuitry, with the data being read from or written to the cells
5   along bitlines using sense amp circuits.

Fig. 1 illustrates a 1T/1C FERAM cell 10 including a transistor 12 and a ferroelectric cell capacitor 14. A bottom electrode of the cell capacitor 14 is connected to a first source/drain terminal 15 of the transistor 12 and the other capacitor electrode is coupled to a plateline or driveline 20. Data is read from the
10   cell 10 by applying a signal to the gate 16 of the transistor 12 along a corresponding wordline WL, thereby connecting the bottom electrode of the ferroelectric capacitor 14 to the other transistor source/drain at a bitline 18. A pulse signal is applied to the plateline 20, where the potential on the bitline 18 is the capacitor charge divided by the bitline capacitance. The capacitor charge is
15   dependent upon the pre-existing bi-stable polarization state of the ferroelectric material in the capacitor 14, wherein the bitline potential can have two distinct values. A sense amplifier (not shown) is connected to the bitline 18 to detect the voltage associated with a logic value of either 1 or 0. Because such a read operation is destructive, the cell data is then rewritten back to the memory cell
20   10.

Fig. 2 illustrates a 2T/2C memory cell 30 in a memory array coupled to a complementary pair of bitlines 32 and 34, where the cell 30 comprises cell transistors 36 and 38 and ferroelectric cell capacitors 40 and 42. The first transistor 36 couples the bitline 32 with a first ferroelectric capacitor 40, and the
25   second transistor 38 couples the complementary bitline 34 to a second ferroelectric capacitor 42. The first and second capacitors 40 and 42 have a common plateline 44 to which a signal is applied for polarizing the capacitors 40 and 42 during read and write operations. For a write operation, the transistors 36 and 38 are enabled *via* a wordline 46 to couple the capacitors 40 and 42 to the
30   complementary logic levels on the bitlines 32 and 34 corresponding to a logic

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state to be stored in the cell 30. The plateline 44 is pulsed to polarize the capacitors 40, 42 to correspond to the desired logic state. In a read operation, the transistors 36 and 38 are enabled *via* the wordline 46 to couple the information stored in the ferroelectric capacitors 40 and 42 to the complementary

5   bitline pair 32 and 34, and a pulse is applied to the plateline 44. This provides a differential signal across the bitline pair 32 and 34 that is sensed by a sense amplifier (not shown), wherein the sensed signal has a polarity corresponding to the data read from the cell 30.

Ferroelectric memory cells are often fabricated in stand-alone memory

10   integrated circuits (ICs) and/or in logic circuits having on-board non-volatile memory (*e.g.*, microprocessors, microcontrollers, DSPs, communications chips, etc.). The ferroelectric memory arrays are typically constructed in a device wafer along with CMOS logic circuits, wherein the cell transistors are often formed concurrently with logic transistors in the device, and the ferroelectric capacitors

15   are constructed in a capacitor layer above the wafer substrate. For example, the construction of the ferroelectric cell capacitors may be integrated into a CMOS fabrication process flow after transistor formation (*e.g.*, after 'front-end' processing), and before the metalization or interconnection processing (*e.g.*, before 'back-end' processing). However, many back-end processing steps

20   include hydrogen, for example, in forming trench etch-stop layers, etch clean operations, copper sintering, and other process steps during metalization. This process hydrogen diffuses into the ferroelectric cell capacitors, causing degradation in the electric properties of the ferroelectric memory cells, including degraded switched polarization. In addition, hydrogen can degrade the

25   performance of transistors in the semiconductor device, for example, causing fixed oxide charge and interface traps at the interface between the transistor gate dielectric and the underlying silicon, leading to negative bias temperature instability (NBTI). This results in reduced drain saturation current (Idsat) and an increase in the transistor threshold voltage (Vsat). Consequently, there is a need

30   for hydrogen barriers and fabrication techniques for protecting ferroelectric

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capacitors and transistors against hydrogen in back-end and other fabrication processing.

SUMMARY OF THE INVENTION

5   The following presents a simplified summary in order to provide a basic understanding of one or more aspects of the invention. This summary is not an extensive overview of the invention, and is neither intended to identify key or critical elements of the invention, nor to delineate the scope of the invention. The summary is provided, rather, to present one or more concepts of the invention in

10   a simplified form as a prelude to the more detailed description that is presented later.

       The present invention relates to hydrogen diffusion barriers for protecting ferroelectric capacitors against hydrogen diffusion in semiconductor devices. One such barrier comprises nitrided aluminum oxide as well as one or more

15   overlying silicon nitride layers. Another hydrogen barrier comprises aluminum oxide formed over the ferroelectric capacitor, with two or more silicon nitride layers formed over the aluminum oxide, wherein the second silicon nitride layer comprises a low silicon-hydrogen SiN material. These new hydrogen barrier structures have been found to facilitate improved ferroelectric capacitor

20   performance with respect to switched polarization compared with conventional techniques in which a single aluminum oxide layer was used.

       In accordance with one aspect of the invention, methods are provided for fabricating semiconductor devices and hydrogen barriers thereof, in which a multilayer hydrogen barrier is formed along at least a portion of a side of a

25   ferroelectric capacitor, where the multilayer hydrogen barrier comprises nitrided aluminum oxide and silicon nitride. The nitrided aluminum oxide may be formed by any suitable process, and may be wholly or partially nitrided after formation of aluminum oxide, or may be initially formed as nitrided aluminum oxide. Nitridation of deposited aluminum oxide may be accomplished by plasma

30   nitridation, thermal nitridation, or other nitridation processing, wherein nitridation

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of deposited aluminum oxide may, but need not, be performed *in-situ* with formation of silicon nitride material over the nitrided aluminum oxide. The silicon nitride can be any suitable single or multi-layer silicon and nitrogen containing material or materials, formed over at least a portion of the aluminum oxide using

5   any suitable deposition process or processes. In one implementation, a high density plasma deposition process is employed to form a first silicon nitride layer over at least a portion of the aluminum oxide material, and a PECVD or other deposition process is performed to deposit a silicon nitride layer over at least a portion of the first silicon nitride layer, where the second silicon nitride layer

10   comprises a low silicon-hydrogen SiN material.

In accordance with another aspect of the invention, a method is provided for fabricating semiconductor devices and hydrogen barriers therefor, in which an aluminum oxide material is formed along at least a portion of a side of a ferroelectric capacitor, and a first silicon nitride layer is formed over at least a

15   portion of the aluminum oxide material. The method further comprises forming a second silicon nitride layer over at least a portion of the first silicon nitride layer, in which the second silicon nitride layer comprises a low silicon-hydrogen SiN material.

According to yet another aspect of the invention, semiconductor devices

20   and hydrogen barriers thereof are provided, wherein the hydrogen barrier comprises a nitrided aluminum oxide material formed along at least a portion of a side of the ferroelectric capacitor, as well as a silicon nitride layer formed over the nitrided aluminum oxide. The silicon nitride can be a single or multi-layer structure, and may comprise a low silicon-hydrogen SiN material. In one

25   example, first and second silicon nitride layers are provided over the nitrided aluminum oxide, wherein the second silicon nitride includes low silicon-hydrogen SiN material.

In accordance with still another aspect of the invention, semiconductor devices and hydrogen barriers thereof are provided, wherein the hydrogen

30   barrier comprises an aluminum oxide material formed along at least a portion of a

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side of a ferroelectric capacitor, a first silicon nitride layer formed over at least a portion of the aluminum oxide material, and a second silicon nitride layer formed over at least a portion of the first silicon nitride layer, the second silicon nitride layer comprising a low silicon-hydrogen SiN material.

5   The following description and annexed drawings set forth in detail certain illustrative aspects and implementations of the invention. These are indicative of but a few of the various ways in which the principles of the invention may be employed.

10   **BRIEF DESCRIPTION OF THE DRAWINGS**

Figs. 1 and 2 are schematic diagrams illustrating exemplary 1T/1C and 2T/2C FERAM memory cells, respectively;

Fig. 3 is a flow diagram illustrating an exemplary method of fabricating a semiconductor device with a hydrogen diffusion barrier in accordance with one or

15   more aspects of the present invention;

Fig. 4A is a partial flow diagram illustrating fabrication of one exemplary hydrogen barrier in the method of Fig. 3;

Fig. 4B is a partial flow diagram illustrating fabrication of another exemplary hydrogen barrier in the method of Fig. 3;

20   Fig. 4C is a partial flow diagram illustrating fabrication of still another exemplary hydrogen barrier in the method of Fig. 3;

Figs. 5A-5J are partial side elevation views in section illustrating an exemplary semiconductor device having a multilayer hydrogen barrier with nitrided aluminum oxide and low Si-H silicon nitride layers in accordance with the

25   invention undergoing fabrication processing generally according to the method of Figs. 3 and 4A;

Figs. 5K-5M are partial side elevation views in section illustrating another exemplary semiconductor device having a multilayer hydrogen barrier with aluminum oxide, a first silicon nitride layer, and a second silicon nitride layer

30   comprising low Si-H silicon nitride material in accordance with the invention

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undergoing fabrication processing generally according to the method of Figs. 3 and 4B;

Figs. 5N-5Q are partial side elevation views in section illustrating another exemplary semiconductor device having a multilayer hydrogen barrier with nitrided aluminum oxide, a first silicon nitride layer, and a second silicon nitride layer comprising low Si-H silicon nitride material in accordance with the invention undergoing fabrication processing generally according to the method of Figs. 3 and 4C;

Fig. 6 is an exemplary Fourier Transform Infrared (FTIR) spectra plot illustrating infrared absorbance or absorption for a low silicon-hydrogen SiN material layer in accordance with the invention;

Fig. 7 is a portion of the exemplary FTIR plot of Fig. 6, illustrating one possible technique for determining a figure of merit for a low silicon-hydrogen SiN material layer in accordance with the invention; and

Figs. 8A and 8B are FTIR spectra plots illustrating infrared absorbance for conventional high silicon-hydrogen SiN layers.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will now be described with reference to the attached drawing figures, wherein like reference numerals are used to refer to like elements throughout, and wherein the illustrated structures are not necessarily drawn to scale. The invention provides semiconductor devices with improved hydrogen diffusion barriers and fabrication methods thereof, in which nitrided aluminum oxide materials and multi-layer silicon nitride structures are employed separately or in combination to protect ferroelectric capacitors and underlying transistors against back-end process hydrogen diffusion. The inventors have appreciated that operational properties of ferroelectric materials and/or transistor devices may be severely degraded by exposure to hydrogen during processing of semiconductor devices, including back-end processing found in many CMOS integration schemes. The inventors have found that nitrided aluminum oxide and

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low silicon-hydrogen SiN films operate as a barrier to hydrogen diffusion, and therefore may be employed to protect ferroelectric capacitors and/or MOS transistors from hydrogenating processes during semiconductor device fabrication.

5   Referring now to Figs. 3, 4A-4C, and 5A-5Q, several exemplary implementations of the invention are hereinafter illustrated. Figs. 3, 4A and 5I-5J depict a method 50 for fabricating a semiconductor device and an exemplary device 102 undergoing fabrication processing according to the method 50, with ferroelectric capacitors and a multi-layer hydrogen barrier comprising nitrided

10   aluminum oxide and a low Si-H silicon nitride. Figs. 4B, 4C, and 5K-5Q depict techniques for forming various alternative hydrogen barriers in the method 50 within the scope of the invention, as illustrated and described further below. While the method 50 is illustrated and described below as a series of acts or events, it will be appreciated that the present invention is not limited by the

15   illustrated ordering of such acts or events. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein, in accordance with the invention. In addition, not all illustrated steps may be required to implement a methodology in accordance with the present invention. Furthermore, the methods according to

20   the present invention may be implemented in association with the fabrication of devices illustrated and described herein, such as the exemplary device 102 in Figs. 5A-5Q, as well as in association with other semiconductor devices and hydrogen barrier structures not illustrated.

The invention may be employed in association with semiconductor

25   devices having ferroelectric capacitors fabricated with any ferroelectric materials, including but not limited to PZT. In addition, the invention may be employed in conjunction with ferroelectric memories using any cell types and array architectures including but not limited to 1T-1C, 2T-2C, or other cell types organized in folded-bitline, open-bitline, chain-FRAM, or other array

30   configurations. In addition, while one or more exemplary semiconductor devices

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are illustrated and described herein with ferroelectric capacitors formed in a dielectric layer or level (*e.g.*, capacitor level) after front-end contact formation and prior to formation of overlying metalization levels, the invention may be employed in devices where ferroelectric capacitors are formed at any level in a multi-level

5   semiconductor device design. Furthermore, the invention may be employed in semiconductor devices fabricated on or in any type of semiconductor body, including but not limited to silicon substrates and SOI wafers. In this regard, the invention is not limited to the examples illustrated and described herein, and all variant implementations providing multi-layer hydrogen barriers with nitrided

10   aluminum oxide and/or low Si-H silicon nitride materials are contemplated as falling within the scope of the present invention and the appended claims.

Referring initially to Figs. 3, 4A, and 5A-5J, the method 50 begins at 52 in Fig. 3, wherein front-end processing is performed at 54, including formation of transistors for the ferroelectric memory cells and transistors and other electronic

15   components for other circuits within the device, using any suitable materials and processing steps. Fig. 5A illustrates an exemplary semiconductor device 102 following such front-end processing in which cell transistors have been formed on or in a semiconductor body 104 prior to fabrication of a poly metal dielectric (PMD) level. The device 102 includes a semiconductor body 104 (*e.g.*, silicon

20   substrate, SOI wafer, etc.) in which transistor source/drains 106 are formed in active regions separated by STI or LOCOS isolation structures 108, and wherein gate structures 110 are formed over channel regions of the substrate 104 as part of conductive polysilicon wordline structures for a ferroelectric memory array. MOS type cell transistors are thus formed by the gates 110 and the source/drains

25   106, wherein the source/drains 106 are formed by doping portions of active regions in the substrate, and wherein the source/drain 106 coupled with a memory array bitline (*e.g.*, the middle source/drain 106 in Figs. 5A-5J) is shared between adjacent transistors in the illustrated example.

At 56, an initial inter-level or inter-layer dielectric (ILD) 114 is formed over

30   the cell transistors using any suitable dielectric material and deposition process,

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where the initial ILD is referred to herein as a poly metal dielectric (PMD). Conductive contacts 116 are formed through the PMD at 56 to provide electric connection to the transistor bitline source/drains (e.g., source/drain 12 in Fig. 1 above), as well as to the source/drains for connection with subsequently formed

5   ferroelectric capacitors (e.g., source/drain 15 in Fig. 1). Any suitable etching and contact formation steps and materials may be employed at 56 within the scope of the invention. As illustrated in Fig. 5B, a poly metal dielectric (PMD) layer 114 is formed over the transistors and the substrate 104, through which conductive contacts 116 are formed for interconnection of the source/drain terminals 106,

10   where the contacts 116 may be formed of any conductive material or materials, such as tungsten or the like.

Ferroelectric capacitors are then formed over the PMD at 58 and 60 (Figs. 5C and 5D). Ferroelectric capacitor layers are formed at 58 over the PMD dielectric and the contacts, including formation of upper and lower conductive

15   capacitor electrode or plate layers and a ferroelectric material layer between the electrode layers, using any suitable conductive and ferroelectric materials and deposition processes. In Fig. 5C, capacitor layers are deposited, including upper and lower conductive electrode or plate layers 118b and 118a, respectively, with a ferroelectric material layer 120 formed between the electrode layers 118. The

20   capacitor electrodes 118 may be formed of any suitable material or combination of multiple layers of materials. In one example, a diffusion barrier is first created comprising TiN formed over the PMD dielectric 114 and the tungsten contacts 116 via chemical vapor deposition (CVD) with a TiAlN film or a TiAlON being deposited thereover using a physical vapor deposition (PVD) or other process.

25   The bottom electrode material 118a is then formed over the diffusion barrier, for example, comprising any conductive material such as Pt, Pd, PdOx, IrPt alloys, Au, Ru, RuO_x, $(Ba,Sr,Pb)RuO_3$, $(Sr,Ba,Pb)IrO_3$, Rh, RhO_x, $LaSrCoO_3$, $(Ba,Sr)RuO_3$, $LaNiO_3$, etc., or any stack or combination thereof.

Ferroelectric material 120 is then deposited over the lower electrode

30   material 118a using any appropriate deposition techniques such as metal organic

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chemical vapor deposition (MOCVD) using any suitable ferroelectric materials, including but not limited to $Pb(Zr,Ti)O_3$ PZT (lead zirconate titanate), doped PZT with donors (Nb, La, Ta) acceptors (Mn, Co, Fe, Ni, Al) and/or both, PZT doped and alloyed with $SrTiO_3$, $BaTiO_3$ or $CaTiO_3$, strontium bismuth tantalate (SBT)

5   and other layered perovskites such as strontium bismuth niobate tantalate (SBNT) or bismuth titanate, $BaTiO_3$, $PbTiO_3$, Bi_2TiO_3, etc. The top electrode material 118b may be a single layer or a multi-layer conductive structure such as IrO_x, RuO_x, RhO_x, PdO_x, PtO_x, AgO_x, $(Ba,Sr)RuO_3$, $LaSrCoO_3$, $LaNiO_3$, $YBa_2Cu_3O_{7-x}$ with a noble metal layer thereover, wherein the layers 118 and 120

10   may be formed to any desired thickness in accordance with the invention.

The capacitor layers are then patterned at 60, for example, using suitable masking and etching steps to define ferroelectric capacitor structures having first and second conductive electrodes and a ferroelectric material disposed between the electrodes. The ferroelectric capacitor material layers 118 and 120 are

15   patterned in Fig. 5D using masking and etch processes (not shown) to define the ferroelectric capacitor structures C_{FE} having any desired size (area) and shape. In the exemplary array configuration of the device 102, the first contacts 116 couple the lower capacitor electrodes 118a with a first source/drain 106 of the cell transistors, and the shared source/drain is coupled with another contact 116

20   for connection with a subsequently formed bitline structure for reading and writing data.

A multi-layer hydrogen barrier is then formed at 62 above the ferroelectric capacitors to prevent or inhibit hydrogen diffusion into the ferroelectric material 120 and/or the underlying transistors in subsequent (e.g., back-end) processing

25   of the device 102. In accordance with one aspect of the invention, the hydrogen barrier is formed with a nitrided aluminum oxide layer, as well as one or more overlying silicon nitride layers. Fig. 4A illustrates a method 62a for fabricating an exemplary hydrogen barrier at 62 in Fig. 3, and Figs. 5E-5I illustrate the exemplary device 102 undergoing processing to form the multi-layer hydrogen

30   barrier generally according to the method 62a of Fig. 4A.

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At 80 in Fig. 4A, a first hydrogen barrier layer is formed over the patterned ferroelectric capacitor structures by depositing aluminum oxide (AlOx in Figs. 5E and 5G) over the ferroelectric capacitors using a deposition process 113, including formation of aluminum oxide along at least a portion of the sides of the

5   ferroelectric capacitors C_{FE}. In one example, the process 113 is a physical vapor deposition (PVD) process that forms an aluminum oxide layer AlOx having a thickness of about 400 Å. In another implementation, an atomic layer deposition (ALD) process 113 is used to deposit the AlOx layer to a thickness of about 100-200 Å. Other aluminum oxide materials having aluminum and oxygen contents

10   and other deposition processes are possible within the scope of the invention, where aluminum oxide material AlOx is formed along at least a portion of one or more sides of the ferroelectric capacitors C_{FE}.

At 82 in Fig. 4A, the deposited aluminum oxide AlOx is nitrided. Figs. 5F and 5H illustrate performance of an exemplary nitridation process 115 that

15   introduces nitrogen into all or a portion of the deposited aluminum oxide AlOx, thereby forming a nitrided aluminum oxide (N-AlOx in Fig. 5F). A nitrided aluminum oxide material within the scope of the invention includes aluminum oxide in which at least a portion of the aluminum oxide material has a non-zero nitrogen content, wherein all stoichiometric variations of such materials are

20   contemplated as falling within the scope of the invention and the appended claims. In one possible structure, a portion of the nitrided aluminum oxide is substantially nitrogen free and an upper or outer portion thereof includes nitrogen, such as aluminum oxynitride, as illustrated in Fig. 5H. Other implementations are possible in which nitrogen is provided substantially

25   throughout the AlOx material layer, and may even be introduced into portions of the ferroelectric capacitor layers 118 and/or 120, wherein all such variant implementations are contemplated as falling within the scope of the invention.

Any suitable nitridation process 115 can be performed at 82 in accordance with the present invention, including but not limited to plasma nitridation and/or

30   nitrogen bake processes 115. In one implementation, a plasma nitridation

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process 115 is performed that exposes at least a portion of the aluminum oxide material AlOx to a nitrogen-containing plasma, at a temperature of about 375 degrees C for about 4 minutes at 1500-3000 Watts RF power. While not wishing to be tied to any particular theory, plasma nitridation processes 115, particularly

5   where relatively higher power is used, are believed to remove or expel some of or more of the moisture from the AlOx than nitrogen bake processes, and/or are believed to form more of an aluminum nitride configuration in at least a portion of the AlOx material, where such implementations have been found to operate as a good barrier against hydrogen diffusion. Any nitrogen-containing plasma may be

10   employed in the plasma nitridation processes 115, including but not limited to nitrogen plasma or nitrous oxide (N_2O) based plasmas, which are believed to expel more hydrogen-oxygen (H-O) ions from the AlOx material than nitrogen bake implementations.

       Nitrogen bake processes 115 are also possible, wherein the wafer is

15   heated in a nitrogen-containing ambient, for example, at about 400 degrees C for about 3 minutes in an ambient that contains N_2, N_2O, or other nitrogen containing environment. In one possible alternative, the nitrogen bake 115 can be performed *in-situ* with subsequent formation (*e.g.*, deposition) of a silicon nitride layer over the AlOx or N-AlOx layer. Other possible implementations are

20   possible within the scope of the invention, for example, wherein nitrided aluminum oxide material N-AlOx (*e.g.*, wholly or partially nitrided aluminum oxide, such as aluminum oxynitride or other material having non-zero aluminum, oxygen, and nitrogen contents) is formed in a single step, wherein the steps 80 and 82 in Fig. 4A (and in Fig. 4C below) may be a single act. The inventors have

25   found that nitriding all or a portion of the AlOx material improves the device performance with respect to ferroelectric capacitor switched polarization, either with a single SiN layer, or in combination with the multi-layer silicon nitride structures described below.

       In addition, the inventors have appreciated that formation of a single or

30   multi-layer silicon nitride (*e.g.*, materials having both silicon and nitrogen

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contents, such as Si_3N_4 or stoichiometric variants thereof, referred to as SiN hereinafter) over the nitrided aluminum oxide advantageously helps to inhibit hydrogen diffusion, leading to improved switched polarization performance in ferroelectric devices. In general, any single or multi-layer silicon nitride material

5   may be formed over the nitrided aluminum oxide using any suitable processes and materials in accordance with the invention. In this regard, although the first barrier layer (e.g., N-AlOx) ideally operates to inhibit the diffusion of hydrogen into the underlying ferroelectric material, the inventors have appreciated that the formation of a low silicon-hydrogen SiN layer 112 over the nitrided AlOx aids in

10   preventing or mitigating hydrogen related performance degradation of the ferroelectric capacitors and the transistors.

In the example of Figs. 4A and 5A-5J, a SiN material 112 is formed at 84 over the nitrided AlOx (e.g., layer 112 formed via deposition process 111 in Fig. 5I), having a low Si-H content. In other possible implementations of the present

15   invention, multiple SiN materials are formed over the AlOx, as described in greater detail below. In the example of Fig. 5I, the low silicon-hydrogen SiN layer 112 is deposited to any desired thickness, such as 200-1000 Å, preferably about 500 Å, using any suitable deposition process 111. The process 111 is preferably a plasma enhanced chemical vapor deposition (PECVD) process employing fairly

20   low ammonia flow (NH_3) and high N_2 flow to provide both a conformal low silicon-hydrogen SiN layer 112, and relatively few, if any, silicon-hydrogen bonds, thereby protecting the ferroelectric transistor C_{FE} from hydrogen associated with subsequent fabrication processing and thermally dissociated hydrogen.

In one example, the PECVD process 111 is performed in Fig. 5I to form a

25   silicon nitride layer 112 over at least a portion of the nitrided aluminum oxide N-AlOx, where the layer 112 comprises a low silicon-hydrogen SiN material having a Fourier Transform Infrared (FTIR) figure of merit value of about 0.05 or less. The FTIR figure of merit is calculated as (Si-H absorbance) / (N-H absorbance x 1.4). In other preferred implementations, the low silicon-hydrogen SiN material

30   has an FTIR figure of merit value of about 0.04 or less, about 0.03 or less in

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another example. In the illustrated device 102, moreover, the low Si-H SiN layer 112 also may operate as an etch-stop material in forming contact openings in a subsequently deposited ILD material.

The inventors have appreciated that conventional silicon nitride materials

5   used as etch stop layers and diffusion barriers typically have a non-zero hydrogen content (*e.g.*, and thus may be more accurately represented as $Si_xN_yH_z$), where the hydrogen content is contained primarily in Si-H bonds and to a lesser extent N-H bonds. The hydrogen in conventional high silicon-hydrogen SiN films tends to dissociate from the SiN material during thermal processing of a

10   device wafer, where the dissociated hydrogen can further exacerbate degradation of the ferroelectric capacitors and transistors. In this regard, the inventors have further appreciated that the Si-H bonds in a SiN material are of lower bond energy (*e.g.*, about 3.34 eV) than are the N-H bonds (*e.g.*, about 4.05 eV). It is therefore believed that hydrogen in the low Si-H SiN films (*e.g.*, layer

15   112) of the present invention will have a lower tendency to dissociate than in conventional SiN (*e.g.*, high silicon-hydrogen SiN) films in which the hydrogen content is largely bonded with silicon.

The present invention provides low silicon-hydrogen SiN barriers at one or more locations above the ferroelectric capacitors, alone or in combination with

20   hydrogen barriers between the transistors and the ferroelectric capacitors, wherein the barriers may also, but need not, function as etch stop layers. The employment of one or more low silicon-hydrogen SiN layers facilitates integration of ferroelectric cell capacitor fabrication in conjunction with existing back-end interconnect (*e.g.*, metalization) processing, while reducing or mitigating

25   hydrogen-related ferroelectric and transistor degradation in stand-alone memory products or devices having embedded ferroelectric memory. The low silicon-hydrogen SiN materials of the present invention, while having some hydrogen content, are believed to have the hydrogen primarily bonded to nitrogen, with little or no hydrogen bonded to silicon, as expressed by an FTIR figure of merit

30   value of about 0.05 or less, where the FTIR figure of merit is calculated as (Si-H

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absorbance / (N-H absorbance x 1.4)), as illustrated and described further below with respect to Figs. 6-8B. Any figure of merit may be used in accordance with this aspect of the invention, which quantifies the relative amounts of silicon bonded hydrogen and nitrogen bonded hydrogen.

5   The low silicon-hydrogen SiN material 112 is preferably formed at 84 using a plasma enhanced chemical vapor deposition (PECVD) process 111 having relatively high nitrogen (N_2) gas flow, and relatively low ammonia (NH_3) flow, so as to create the material 112 having hydrogen content confined primarily to nitrogen-hydrogen bonds. In one example, the process 111 employs an N_2

10   flow of about 10,000 sccm or more, such as about 14,000 sccm or more, with an NH_3 flow of about 1,000 sccm or less, such as about 750 sccm or less. The following table 1 provides process parameters for several exemplary implementations of a PECVD deposition process 111 that may be employed in forming a low silicon-hydrogen layer 112 (e.g., at 84 in Figs. 4A-4C) within the

15   scope of the invention.

Table 1:

Parameter	Recipe I	Recipe II	Recipe III
N_2 flow sccm	14,000	4,500	1,500
SiH_4 flow sccm	150	50	100
NF_3 flow sccm	0	0	50
NH_3 flow sccm	750	250	700
HFRF watts	700	1000	1000
LFRF watts	100	300	300
Pressure Torr	2.25	2.7	2.8
Temp deg. C	400	400	400
F.O.M. Si-H/1.4N-H	0.00	0.04	0.02

The low silicon-hydrogen SiN layer 112 has a low FTIR figure of merit value, for example, about 0.05 or less, calculated as a ratio of the FTIR spectra

20   areas for Si-H and N-H with appropriate scaling (Si-H absorbance / (N-H

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absorbance x 1.4)). The low figure of merit indicates the relatively low amount of Si-H bonds within the SiN material compared to the amount of N-H bonds, wherein the nitrogen bonded hydrogen is less likely to dissociate and cause degradation of the ferroelectric capacitors and or transistors in the semiconductor

5 device. The low silicon-hydrogen SiN layer 112, moreover, may be deposited using a plasma enhanced chemical vapor deposition (PECVD) process employing high nitrogen and low ammonia flows to provide a highly conformal deposition thickness. The conformal deposition thickness facilitates operation of the SiN layer as an effective hydrogen barrier to protect ferroelectric material and

10 transistor gate interfaces, particularly along the sidewalls of a somewhat vertical ferroelectric capacitor stack. The low silicon-hydrogen SiN layer 112 may be formed anywhere above the ferroelectric capacitors, for example, such as directly over the nitrided aluminum oxide or with one or more intervening materials layers therebetween, wherein the low silicon-hydrogen SiN 112 may also operate as an

15 etch stop layer in the capacitor level.

In Fig. 5J, an ILD layer 122 is formed in the capacitor level over the ferroelectric capacitor structures C_{FE}, the bitline contacts 116, the PMD dielectric 114, and the low silicon-hydrogen SiN layer 112, where the ILD material 122 may be silicon dioxide (SiO_2), FSG, or other suitable dielectric. Openings are etched

20 in the dielectric layer 122 using the low silicon-hydrogen SiN layer 112 as an etch stop layer. The openings through the ILD material 122 are then filled with conductive material (e.g., tungsten, copper, etc.) to form conductive via structures 124 for coupling with the upper capacitor plates 118b and the bitline contacts 116 of the capacitor level. The wafer is thereafter planarized (e.g.,

25 using CMP or other techniques), thereby completing the capacitor layer or level in the device 102 as shown in Fig. 5J. Additional ILD dielectric layers (not shown) may thereafter be formed over the ferroelectric capacitor level, and etched to form single and/or dual damascene type openings that are filled with metal (e.g., copper) to complete the metalization in the device 102.

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Compared with conventional aluminum oxide/silicon nitride barriers, the inventors have found that full or partial nitridation of the aluminum oxide may facilitate improved switched polarization performance in ferroelectric memory devices. According to another aspect of the invention, multilayer hydrogen

5   diffusion barriers are provided in which an aluminum oxide layer AlOx (that may, but need not be nitrided) is formed at least partially over the ferroelectric capacitors C_{FE}, with two or more silicon nitride layers formed over the AlOx.

Referring now to Figs. 4B and 5K-5M, another aspect of the invention provides for a multilayer hydrogen barrier with aluminum oxide, a first silicon

10   nitride layer, and a second silicon nitride layer that comprises low Si-H silicon nitride material. The provision of the multiple silicon nitride layers, where at least one comprises low Si-H material, may be employed with any aluminum oxide AlOx as set forth in Figs. 4B and 5K-5M, or in combination with nitrided aluminum oxide N-AlOx, as discussed below with respect to Figs. 4C and 5N-5Q.

15   Fig. 4B illustrates acts 62b for forming a multi-layer hydrogen barrier at 62 in the method 50 of Fig. 3, and Figs. 5K-5M illustrate the exemplary device 102 undergoing hydrogen barrier fabrication processing generally according to the acts of Fig. 4B. At 80 in Fig. 4B, an aluminum oxide layer is formed along at least a portion of the ferroelectric capacitor sides (*e.g.*, AlOx layer formed *via* the

20   process 113 in Fig. 5K), wherein the same deposition process 113 described above or other suitable material formation processing may be employed. At 83, a first silicon nitride material layer 117 is formed over the aluminum oxide AlOx *via* a deposition process 119, as shown in Fig. 5L. In one implementation, the formation of the first silicon nitride 117 at 83 involves performing a high density

25   plasma (HDP) deposition process 119, which forms a SiN material 117 that has relatively high amounts of Si-H over the AlOx layer. In the illustrated example, the process 119 employs silane gas flow of about 40 sccm, argon (Ar) flow of about 250 sccm, N2 MFC flow of about 400 sccm, and a low frequency deposition power setting of about 1850 watts, although any suitable deposition

30   process 119 can be used.

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At 84 in Fig. 4B, a second silicon nitride layer 112 is formed over at least a portion of the first silicon nitride layer 117 *via* the exemplary PECVD process 111 described above or other suitable process, as illustrated in Fig. 5M. The second silicon nitride layer 112 comprises low-silicon-hydrogen SiN material having an

5   FTIR figure of merit value of about 0.05 or less, preferably about 0.04 or less, more preferably about 0.03 or less, wherein the FTIR figure of merit is calculated as (Si-H absorbance) / (N-H absorbance x 1.4). The inventors have found that compared with conventional aluminum oxide/silicon nitride barriers, the use of two SiN layers as shown in Figs. 4B and 5M further improves the switched

10   polarization performance of the underlying ferroelectric capacitors.

Yet another aspect of the invention provides for combination of nitrided aluminum oxide N-AlOx with a multi-layer SiN structure, as shown in Figs. 4C and 5N-5Q. Fig. 4C illustrates acts 62c for forming a multi-layer hydrogen barrier at 62 in the method 50 of Fig. 3, and Figs. 5N-5Q illustrate the exemplary device

15   102 undergoing hydrogen barrier fabrication processing generally according to the acts of Fig. 4C. As illustrated in Figs. 4C and 5N, an aluminum oxide layer AlOx is formed at 80 along at least a portion of the ferroelectric capacitor sides *via* the process 113, wherein the same deposition process 113 described above (*e.g.*, with reference to Figs. 5F and 5H above) or other suitable material

20   formation processing may be employed. In Fig. 5O, the AlOx material is nitrided at 82, using any of the processing described above (*e.g.*, plasma nitridation, nitride bake, or others) to form fully or partially nitrided aluminum oxide N-AlOx over the ferroelectric capacitors C_{FE}.

At 83, a first silicon nitride material layer 117 is formed in Fig. 5P over the

25   nitrided aluminum oxide N-AlOx *via* a deposition process 119 (*e.g.*, HDP process 119 as described above). At 84, a second silicon nitride layer 112 is formed over at least a portion of the first silicon nitride layer 117 *via* the exemplary PECVD process 111 described above or other suitable process, to provide a low Si-H SiN material 112, as illustrated in Fig. 5Q, wherein the total combined thickness of

30   the SiN layers 117 and 112 can be any value, such as about 500-1000 Å in the

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illustrated example. As in the above examples, the silicon nitride layer 112 comprises low-silicon-hydrogen SiN material having an FTIR figure of merit value of about 0.05 or less, preferably about 0.04 or less, more preferably about 0.03 or less, wherein the FTIR figure of merit is calculated as (Si-H absorbance) / (N-H absorbance x 1.4). The inventors have found that the use of two SiN layers formed over a nitrided aluminum oxide as a hydrogen barrier can significantly improve switched polarization performance, in some examples by as much as 200% or more.

Figs. 6-8B further illustrate the advantages of and exemplary techniques for measuring or characterizing the low Si-H silicon nitride materials 112 of the present invention. Fig. 6 illustrates an exemplary FTIR plot 300, showing an infrared absorbance or absorption spectra 302 for a low silicon-hydrogen SiN layer in accordance with the invention (e.g., layer 112 in the device 102 above). Fig. 7 further illustrates a portion of the plot 300 of Fig. 6, showing one possible technique for determining a figure of merit for a low silicon-hydrogen SiN layer in accordance with the invention. Figs. 8A and 8B provide FTIR spectra plots 310 and 320 illustrating infrared absorbance for conventional high silicon-hydrogen SiN layers (e.g., having figures of merit greater than 0.05).

As used herein, the FTIR figure of merit for the low silicon-hydrogen SiN materials of the invention relates the relative amounts of silicon-hydrogen (Si-H) and nitrogen-hydrogen (N-H) in the deposited SiN. It is believed that the hydrogen content of the low silicon-hydrogen SiN materials of the invention has a lower tendency to dissociate than in conventional SiN materials in which the hydrogen content is largely bonded with silicon, because Si-H bonds are of lower bond energy (e.g., about 3.34 eV) than are N-H bonds (e.g., about 4.05 eV).

FTIR spectra may be used to provide a figure of merit (FOM) or value used in ascertaining the relative amounts of silicon-hydrogen (Si-H) and nitrogen-hydrogen (N-H) in a SiN material. FTIR spectroscopy is the study of the interaction of infrared (IR) radiation with a sample, such as a wafer with a deposited SiN layer, to measure the frequencies at which the sample absorbs

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such radiation, as well as the intensity of the absorption. This type of measurement allows identification of the chemical composition of the sample (*e.g.*, of the deposited SiN material), because chemical functional groups, such as SiN, Si-H, N-H, etc., are known to absorb IR radiation at specific frequencies,

5   wherein the intensity of the absorption at a certain frequency or frequency band is related to the concentration of the corresponding component. In typical FTIR spectra plots, such as the exemplary plot 300 in Figs. 6 and 7, the frequency (X axis) is generally depicted in terms of wavenumbers in units of cm^{-1}.

For the exemplary low hydrogen-silicon SiN material corresponding to the

10   Plot 300 in Figs. 6 and 7, a large peak is found, that is centered at around 900 cm^{-1}, corresponding to SiN. It is known that Si-H absorption will appear in the wavenumber range of 2050-2350 cm^{-1}, and that N-H absorption is found in the wavenumber range of 3200-3425 cm^{-1}, as shown by the circled portions of the absorption spectra 302. It is further assumed that Si-H bonds in SiN have about

15   1.4 times the specific absorption of N-H bonds, which is believed to be due to the corresponding difference in bond energies. The absorption intensity at these bands of interest can be quantified in terms of the area under the peaks, which may be computed or calculated using any suitable technique within the scope of the invention. The ratio of the areas for Si-H and N-H is then determined and

20   divided by the scaling factor 1.4 (*e.g.*, Si-H/1.4N-H) to obtain the figure of merit, wherein the low silicon-hydrogen SiN materials of the present invention have an FTIR figure of merit of about 0.05 or less, such as 0.04 or less in one example, and about 0.03 or less in another example.

One possible technique for obtaining the relevant area measurement from

25   the FTIR spectra 302 is illustrated in Fig. 7, wherein a line 304 is drawn beneath the peak (*e.g.*, local maxima) of interest (*e.g.*, N-H in Fig. 7). The wavenumber (*e.g.*, frequency) at which the peak occurs is identified as 'v', and the corresponding intensity value 'I' is identified (*e.g.*, I = -0.092 in this example). A corresponding intensity value I_0 is determined as the intensity of the line 304 at

30   the frequency v (*e.g.*, I_0 = -0.114 in this example). Using these intensity values, a

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third intensity I' is determined as the square root of the product I and I_0 (e.g., I' is the square root of $((-0.092) \times (-0.114)) = 0.1024$ in this example). A line 306 is then drawn parallel to the line 304, so as to intersect the frequency v and the intensity value I'. The frequency values at which this line 306 crosses the spectra

5   302 are subtracted to obtain a value Δv (e.g., = about 110 cm^{-1} in this example). The area corresponding to the N-H peak is then determined as 'A' times Δv, where $A = \log_{10}$ of $I_0/I = 0.0931$, resulting in an area of about 10.243.

A similar technique can be employed to find the area under any peak for Si-H, and the ratio of the areas is divided by 1.4 (e.g., Si-H/1.4N-H) to obtain the

10 FTIR figure of merit. As can be seen in the FTIR spectra 302 in Figs. 6 and 7, most of the hydrogen in the low silicon-hydrogen SiN is involved in N-H bonds, whereby the hydrogen is less likely to dissociate during thermal processing of a semiconductor device wafer. In this manner, the low silicon-hydrogen SiN is less likely to act as a source of hydrogen to ferroelectric capacitors or transistors than

15 are SiN films having high silicon-hydrogen content. Furthermore, the employment of PECVD deposition techniques using high N_2 flow and low ammonia flow for forming the low silicon-hydrogen SiN provides more conformal coverage, particularly along the lateral sidewalls of capacitor and transistor structures, thereby providing a better barrier against hydrogen diffusion than

20 conventional HDP SiN deposition techniques. As seen in Table 1 above, the figure of merit for the exemplary low silicon-hydrogen SiN materials of the invention is about 0.05 or less. This is exemplified in the Plot 300, wherein the spectra curve 302 is basically smooth in the Si-H band of wavenumbers 2050-2350, indicating little or no absorption. Consequently, the material has little or no

25 Si-H, but relatively high amounts of N-H.

Referring also to Figs. 8A and 8B, the inventors have found that conventional high silicon-hydrogen SiN materials typically yield a corresponding FTIR figure of merit of about 0.8 or more. Fig. 8A illustrates a first plot 310 with an FTIR spectra 312 having a significant peak absorbance for the Si-H band at

30 2050-2350 cm^{-1}, and a relatively smaller peak absorbance for the N-H band at

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3200-3425 cm^{-1}. The same is true in Fig. 8B, where a plot 320 is provided for an FTIR spectra 322. In this example, the spectra 322 similarly indicates a high absorbance for Si-H and relatively lower absorbance for N-H, wherein a large amount of hydrogen is contained in weaker Si-H bonds, therefore being more

5   likely to dissociate at temperature, leading to ferroelectric PSW degradation and/or to NBTI problems for device transistors.

While the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended

10   claims. In particular regard to the various functions performed by the above described components or structures (assemblies, devices, circuits, systems, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component or structure which performs the specified function of the described

15   component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary implementations of the invention. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more

20   other features of the other implementations as may be desired and advantageous for any given or particular application. Furthermore, to the extent that the terms "including", "includes", "having", "has", "with", or variants thereof are used in either the detailed description and the claims, such terms are intended to be inclusive in a manner similar to the term "comprising".

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